SPECIFICATIONS

PXIe-6674T

Timing and Synchronization Module for PXI Express

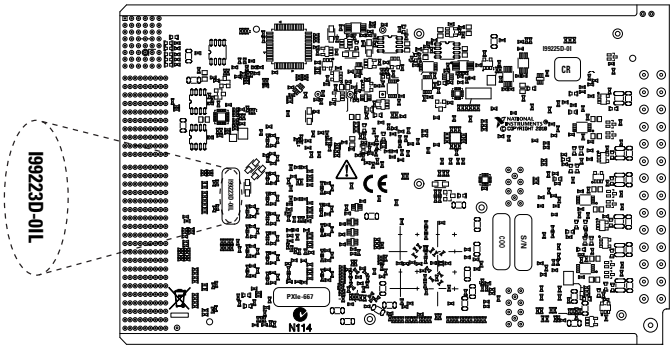
This section lists the system specifications for PXIe-6674T modules. These specifications are typical at 25 °C, unless otherwise stated.

Caution Specifications are subject to change without notice.

Note Some specifications are specific to earlier revisions of the PXIe-6674T module. A label with revision information can be found on the module board as shown in the PXIe-6674T Revision Label figure below.

x denotes all letter revisions of the assembly. Ensure the specifications of interest match the revision that is printed on the label.

Figure 1. PXIe-6674T Revision Label



Definitions

Warranted specifications describe the performance of a model under stated operating conditions and are covered by the model warranty.

Characteristics describe values that are relevant to the use of the model under stated operating conditions but are not covered by the model warranty.

- *Typical* specifications describe the performance met by a majority of models.
- *Nominal* specifications describe an attribute that is based on design, conformance testing, or supplemental testing.

Specifications are *Typical* unless otherwise noted.

PXIe-6674T Specifications Conditions

Specifications are valid at 25 °C unless otherwise noted.

Safety Guidelines

Caution This icon denotes a caution, which advises you to consult documentation where this symbol is marked.

Caution Do not operate the PXIe-6674T in a manner not specified in this document. Product misuse can result in a hazard. You can compromise the safety protection built into the product if the product is damaged in any way. If the product is damaged, return it to NI for repair.

Caution You can impair the protection provided by the PXIe-6674T if you use it in a manner not described in this document.

CLKIN Characteristics

Input coupling	AC
Input impedance	50 Ω, nominal

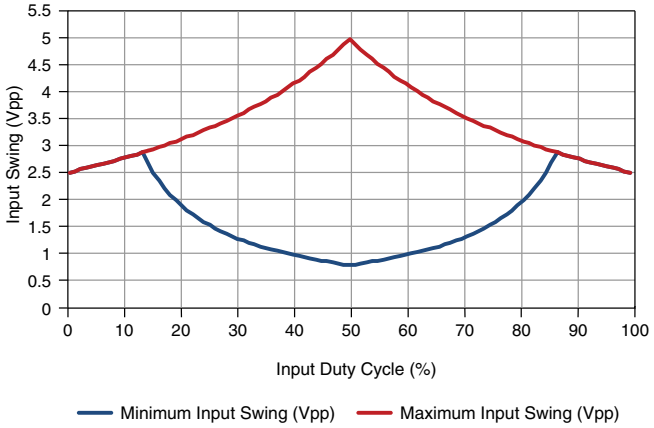
Setting	Attenuation Setting On	Attenuation Setting Off
Attenuation Setting	On (default)	Off
Attenuation Behavior	5:1	1:1
Minimum Input Swing with 50% Duty Cycle[1]	750 mV_{pp}	150 mV_{pp}

[1] A duty cycle other than 50% will increase the minimum input swing. Refer to *Maximum and Minimum Input Swing with Attenuation On* for more information.

Setting	Attenuation Setting On	Attenuation Setting Off
Maximum Input Swing with 50% Duty Cycle[2]	5.0 V_{pp}	1.2 V_{pp}
Absolute Maximum Input Powered On[3]	5.6 V_{pp}	2.8 V_{pp}
Absolute Maximum Input Powered Off[4]	1.5 V_{pp}	

Note Input can be either square wave or sinusoidal.

Figure 2. Maximum and Minimum Input Swing with Attenuation On

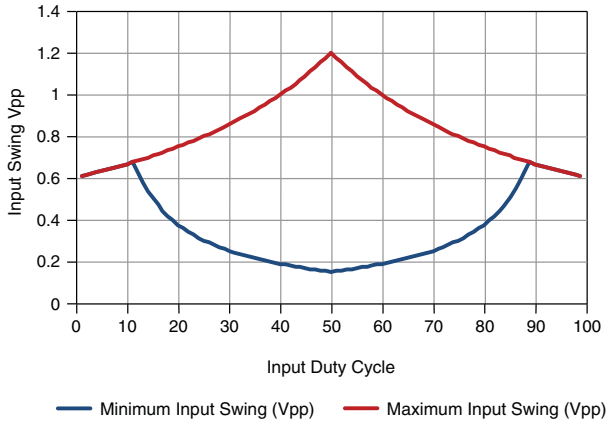


[2] A duty cycle other than 50% will increase the minimum input swing. Refer to *Maximum and Minimum Input Swing With Attenuation Off* for more information.

[3] Operation above the Absolute Maximum Input Powered On may cause damage to the device.

[4] Absolute Maximum Input Powered Off is the maximum input signal amplitude that the device can tolerate before damage might occur while in an unpowered state.

Figure 3. Maximum and Minimum Input Swing With Attenuation Off



Minimum Frequency	1 MHz[5]
Maximum Frequency	
To Clk10PLL	100 MHz
To FPGA	200 MHz
To PXIe-DStarA	1 GHz
ClkIn to PXI_Clk10_In Delay (PLL not used)	
Typical at 25 °C	6.75 ns
Maximum over temperature	14.8 ns

OCXO

Nominal Frequency	10 MHz
Accuracy within 1 year of calibration adjustment within 0 °C to 55 °C operating temperature range [6]	± 80 ppb
Long-term stability	±50 ppb/year
Stability vs temperature	<10 ppb peak-to-peak within 0 °C to 55 °C operating temperature range

[5] The minimum frequency is limited by AC coupling.
[6] After 72 hours of continuous operation.

Tuning Range	±1.5 ppm minimum, ±2 ppm typical, ±4 ppm maximum
Tuning DAC Resolution	16 bits, 0.0625 ppb per step typical
Recommended calibration interval	1 year

Table 1. Typical Phase Noise of the OCXO

Offset	Phase Noise
1 Hz	< -80 dBc/Hz
10 Hz	< -120 dBc/Hz
100 Hz	< -140 dBc/Hz
1 kHz	< -145 dBc/Hz
10 kHz	< -150 dBc/Hz

The following figure shows the phase noise on a representative module. OCXO is routed to the ClkOut SMA, measured in a PXIe-1082 chassis with low fan speed[7]. The integrated jitter from 10 Hz to 1 MHz is 507 fs rms

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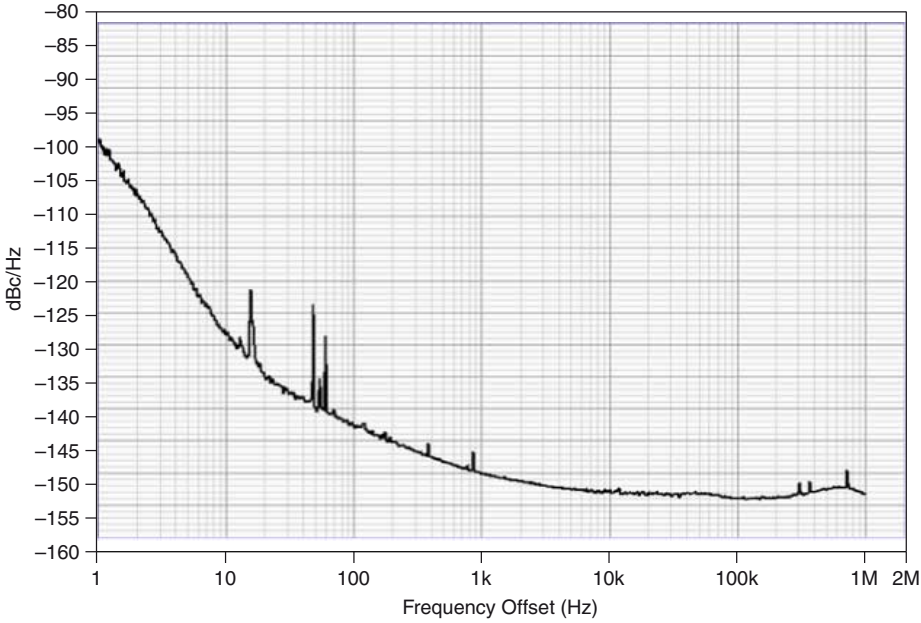
[7] OCXO also driven to PXI_CLK10_IN.

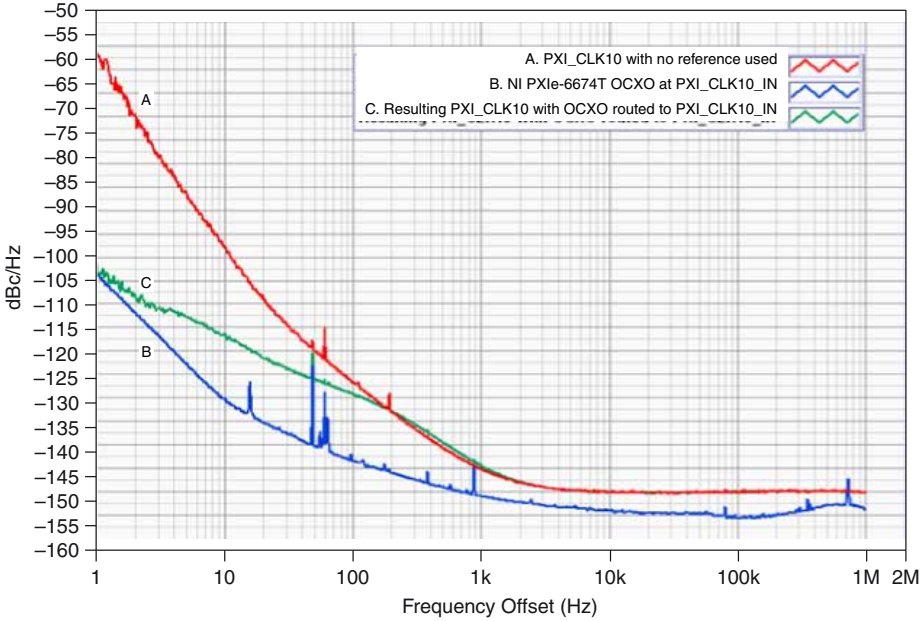
Figure 4. Phase Noise on a Representative Module with OCXO Routed to ClkOut SMA



The following figure shows the phase noise on a representative module of PXI_CLK10 when OCXO is routed to PXI_CLK10_IN,[8] measured in a PXIe-1082 chassis with low fan speed:

[8] The PXIe backplane employs a PLL to phase lock PXI_CLK10 to the signal on PXI_CLK10_IN. As a result, the phase noise of PXI_CLK10 above about 1 kHz offset is unchanged, regardless of reference used.

Figure 5. Phase Noise on a Representative Module of PXI_CLK10 when OCXO is routed to PXI_CLK10_IN



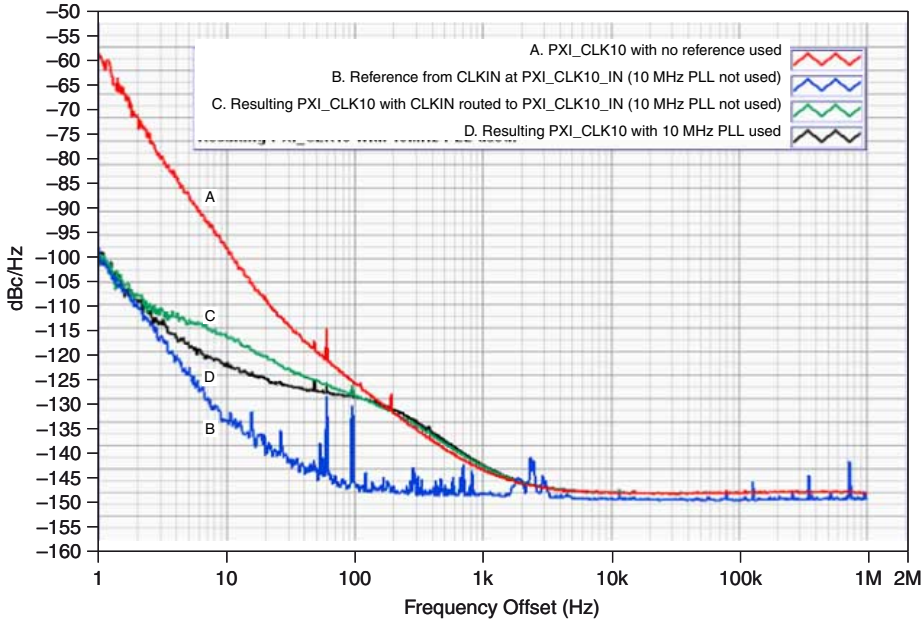
10MHz PLL

Reference Frequency Range (from ClkIn)	1 MHz to 100 MHz, in increments of 1 MHz
Recommended ClkIn Frequency[9]	10 MHz
Reference Frequency Required Accuracy	± 1.5 ppm
Reference Frequency Duty Cycle	40% to 60%
PLL Loop Bandwidth	100 Hz
Maximum PXI_CLK10 Phase Offset	+/- 1 ns

[9] 10 MHz PLL filter is designed for a 10 MHz phase detector frequency. Any other reference frequency will default to a phase detector frequency of 1 MHz resulting in a slight degradation of PLL performance.

The following figure shows the phase noise on a representative module of PXI_CLK10 when CLKIN is routed to PXI_CLK10_IN with and without the 10 MHz PLL, measured in a PXIe-1082 chassis with low fan speed.[10]

Figure 6. Phase Noise on a Representative Module of PXI_CLK10 with CLKIN Routing to PXI_CLK10_IN



ClkOut

	Low Speed ClkOut	High Speed ClkOut
Coupling	AC Coupled	AC Coupled
Expected Termination	50 Ω or high impedance	50 Ω

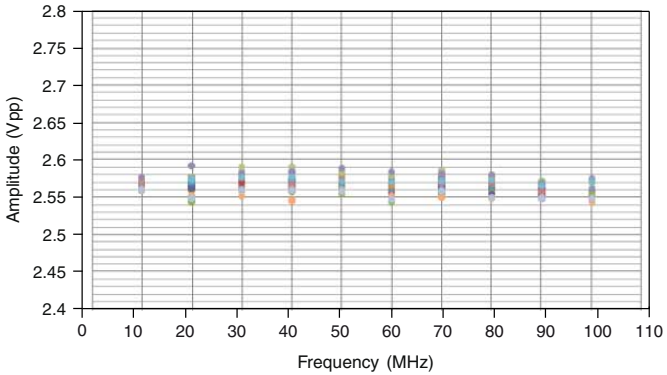
[10] The PXIe backplane employs a PLL to phase lock PXI_CLK10 to the signal on PXI_CLK10_IN. As a result, the phase noise of PXI_CLK10 above about 1 kHz offset is unchanged, regardless of reference used.

	Low Speed ClkOut	High Speed ClkOut
Frequency Range	1 MHz to 50 MHz[11]	1 MHz to 1 GHz[12]
Typical Amplitude	2.57 V_{pp} into 50 Ω, 5 V_{pp} into high Z	800 mV_{pp}
Rising/Falling Edge (20%, 80%)	270 ps, typical	180 ps, typical
Duty Cycle of output with Clock Generation as source	45% to 55%	45% to 55%
Available Sources	PXI_CLK10, 10 MHz OCXO, Clock Generation up to 50 MHz	Clock Generation, PXIe-DStarA Network[13]

PXI_CLK10 to ClkOut Delay	
Typical at 25 °C	20.2 ns
Maximum over temperature	47.75 ns

The following figure shows the typical Low Speed ClkOut Amplitude performance, with a sample size of 19 modules.

Figure 7. Typical Low Speed ClkOut Amplitude Performance



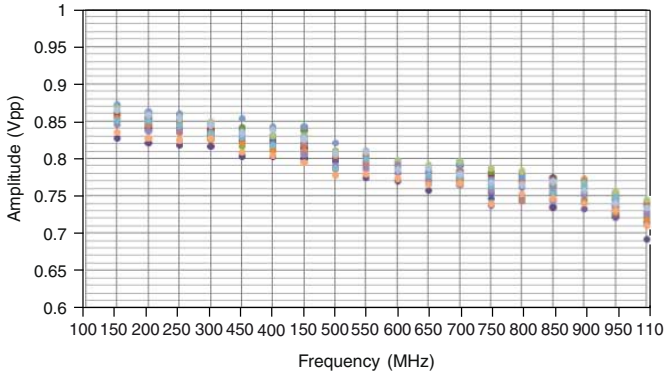
The following figure shows the typical High Speed ClkOut Amplitude performance, with a sample size of 19 modules.

[11] Operation of low speed ClkOut above 50 MHz is possible however NI does not guarantee performance. Use ClkOutLS as the destination terminal to force NI-Sync to use the low speed driver above 50 MHz.

[12] Operation above 1 GHz is possible but NI does not guarantee performance.

[13] Routing PXIe-DStarA to ClkOut requires routing through either Banks 0, 1, or 2.

Figure 8. Typical High Speed ClkOut Amplitude Performance



Clock Generation

Reference Frequency Source[14]	PXIe_Clk100
Base Frequency Resolution (150 MHz to 300 MHz)	2.84217 µHz[15]
Minimum Generated Frequency[16]	
With FPGA divider	0.2794 Hz
Without FPGA divider	4.6875 MHz
Maximum Generated Frequency	1 GHz[17]

Clock Generation Phase Noise Performance

Note All phase noise measurements were made on a Representative Module of various clock generation frequencies routed to ClkOut. All measurements made in an PXIe-1062 chassis with low fan speed and OCXO connected to PXI_Clk10_IN.

[14] Frequency Accuracy is inherited from PXIe_Clk100/PXI_Clk10. Use OCXO for PXIe_Clk100/PXI_Clk10 replacement for improved frequency accuracy and phase noise.

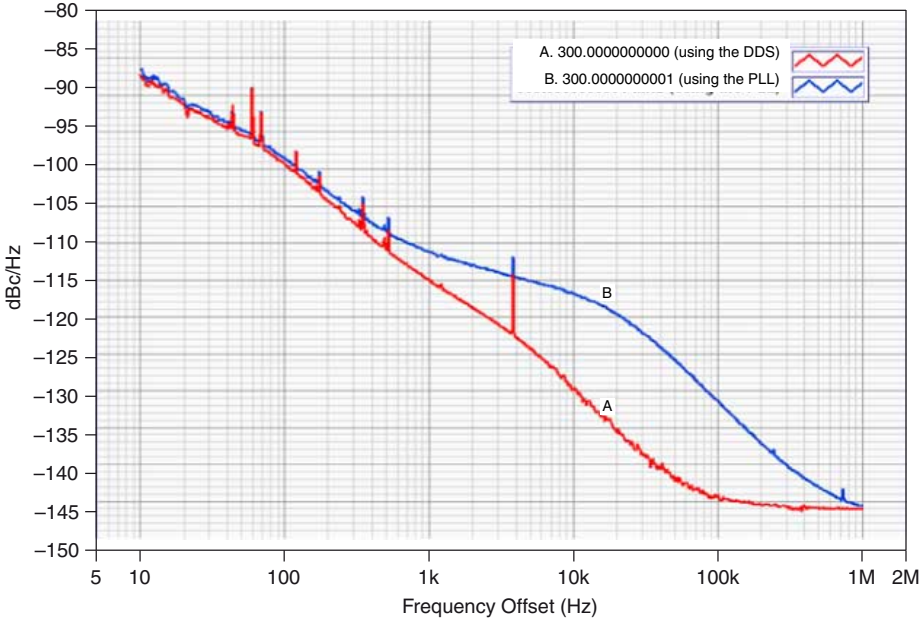
[15] This is the frequency resolution of the DDS used in the Clock Generation circuitry. For Clock Generation frequencies below 150 MHz, this resolution is divided down and for frequencies above 300 MHz, this resolution is multiplied up.

[16] When routed to ClkOut Low Speed or used as a trigger synchronization clock, Clock Generation can be further divided by theFPGA by factors of two up to 24. This extends the Clock Generation range down to 4.6875 MHz/224=.2794 Hz. When routed to ClkOut High Speed the minimum frequency is 4.6875 MHz. Use ClkOutHS as the destination terminal to force NI-Sync to use the low speed driver below 50 MHz. Note that AC coupling on ClkOut limits the minimum frequency which can be used.

[17] Clock Generation can be operated beyond the upper limit; however, NI does not guarantee performance beyond 1 GHz. 2 GHz is the maximum output frequency by design.

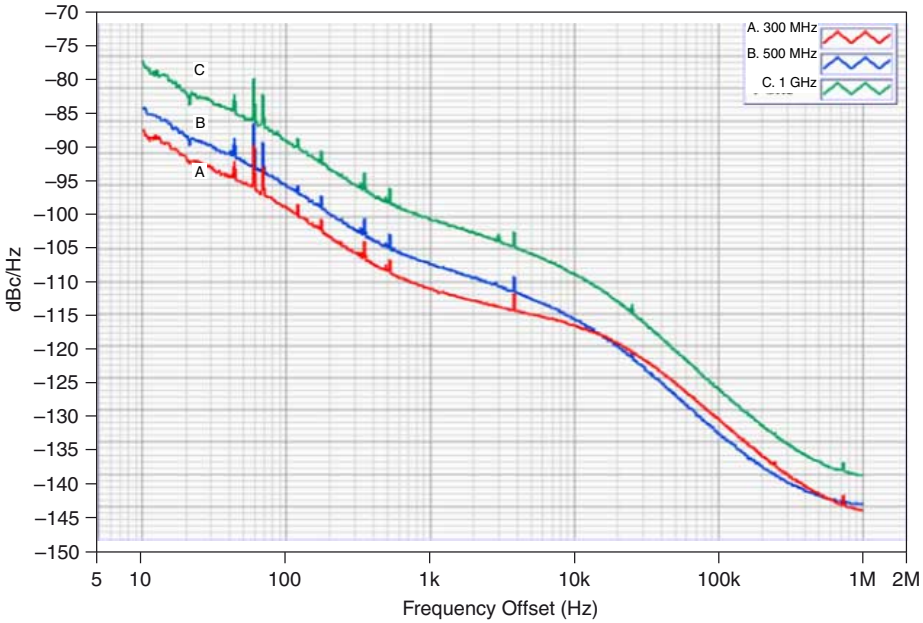
The phase noise performance of the clock generation circuitry varies depending on what elements are used to generate the requested frequency. To generate frequencies above 300 MHz, a PLL is used to multiply the DDS frequency up which results in increased phase noise versus when the DDS is used directly (all frequencies below 300 MHz).

Figure 9. Phase Noise Performance



The following figure shows the phase noise of various frequencies coming from the multiplying PLL.

Figure 10. Phase Noise of Frequencies From the Multiplying PLL



At 50 MHz, NI-Sync software will automatically switch between the high speed and low speed ClkOut drivers[18]. The phase noise performance of these two drivers differs, as shown in the following figure:

[18] Use ClkOutHS as the destination terminal to force NI-Sync to use the high speed driver below 50 MHz.

Figure 11. Phase Noise of Frequencies from DDS

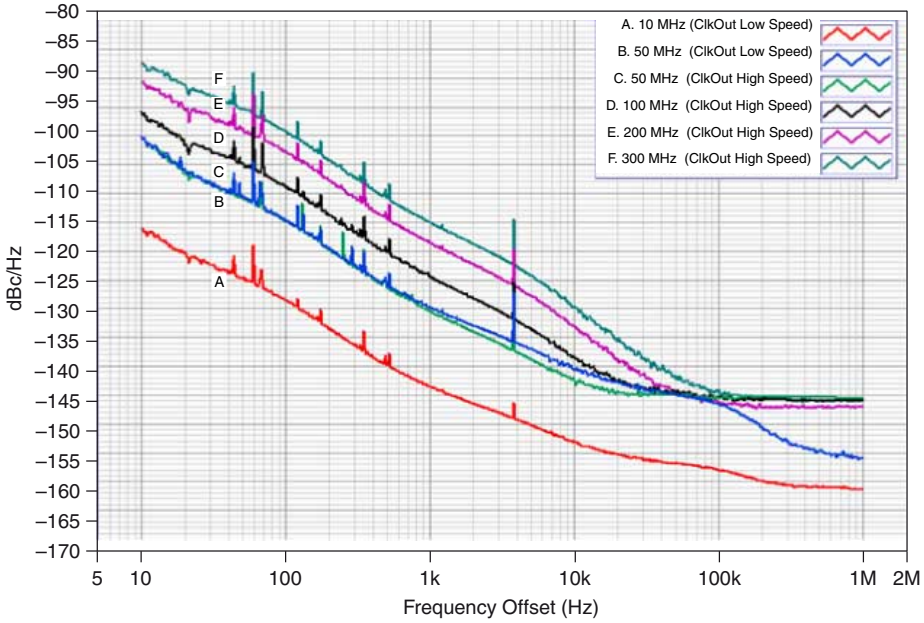
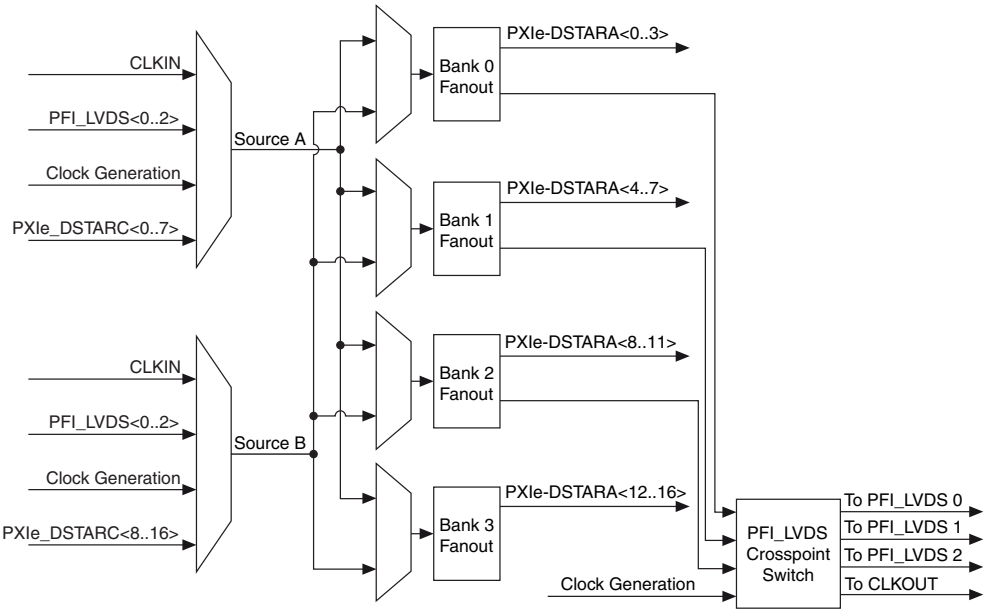


Figure 12. PXIe-DStarA Topology



PXIe-DStarA Maximum Frequency	1 GHz[19]

Table 2. PXIe-DStarA LVPECL Signal Characteristics

	Minimum	Typical	Maximum
Voltage High Output	2.155 V	2.280 V	2.405 V
Voltage Low Output	1.355 V	1.530 V	1.700 V
Rise Time/Fall Time 20%, 80%	125 ps	180 ps	275 ps

ClkIn to PXIe-DStarA Delay	
Typical at 25 °C	4.21 ns
Maximum over temperature	4.36 ns

[19] Maximum Frequency may exceed 1 GHz, however, performance is not guaranteed.

PXIe-DStarA to PXIe-DStarA Skew	
Typical	100 ps
Maximum over temperature	250 ps

Triggers

PFI Single Ended

Table 3. Input Characteristics

Termination Setting	High Impedance	50 Ω
Input Impedance	10kΩ, ± 20%	50 Ω, ± 5%
Input Coupling	DC	DC
Hysteresis	50 mV typical	58 mV typical (Revision C and D)[20], 53 mV typical (Revision E and later)[20]
Adjustable Threshold Range	15 mV to 3.795 V	16.8 mV to 4.25 V (Revision C and D)[20], 15.975 mV to 4.04 V (Revision E and later)[20]
Adjustable Threshold Resolution	15 mV	16.8 mV (Revision C and D)[20], 15.975 mV (Revision E and later)[20]
Adjustable Threshold Error[21]	± 5 mV	± 5 mV
Default Threshold Setting	1.005 V	1.008 V (Revision C and D)[20], 1.006 V (Revision E and later)[20]
Minimum Input Voltage Swing[22]	400 mV_{pp}	450 mV_{pp}
Frequency Range[23]	DC to 150 MHz	DC to 150 MHz
Recommended Maximum Input Voltage Range	0.0 V to 5.0 V	0.0 V to 5.0 V

[20] Ensure that the specifications of interest match the revision label on your board.
[21] PFI Input switching behavior is a function of both the threshold setting and hysteresis.
[22] Input Voltage Swing below 400mV may be possible but performance is not guaranteed.
[23] Operation beyond 150MHz frequency may be possible but performance is not guaranteed.

Table 3. Input Characteristics (Continued)

Maximum Input Voltage Range	–0.5 V to 5.5 V	–0.5V to 5.5 V
PFI Open Circuit Voltage[24]	0.45 V, typical	N/A

Table 4. Output Characteristics

Output Impedance	50 Ω, nominal
Output Coupling	DC
Output Voltage Range into 50 Ω load	0 V to 1.63 V, typical
Output Voltage Range into open load	0 V to 3.22 V, typical
Output Rising/Falling Edge into 50 Ω load	450 ps to 500 ps, 20%–80%, typical
Maximum Output Frequency[25]	DC to 150 MHz

PFI LVDS

Input Characteristics

Minimum Differential Input Voltage	100 mV_{pp}
Recommended Maximum Differential Input Voltage[26]	1 V
Maximum Input Voltage Range[27]	0 V to 4 V
Differential Input Resistance	100 Ω, ± 10%

[24] PFI line will float to 0.45V when configured in high impedance mode with no external signal connected as input.

[25] Operation beyond 150 MHz frequency may be possible but performance is not guaranteed.

[26] Operation with greater voltage swing will not damage the device but performance characteristics are not guaranteed.

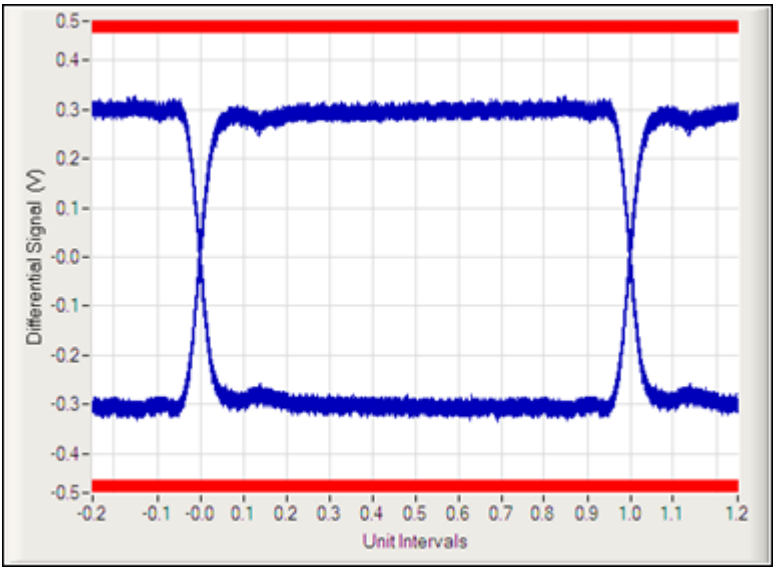
[27] Maximum Input Voltage Range is any combination of input voltage swing and common mode voltage. For example, a 200 mV differential swing with common mode voltage of 100 mV is acceptable as the lowest applied voltage to the input would be 0 V. A 200 mV differential swing with common mode less than 100 mV would cause the applied voltage to fall below 0 V and therefore would not be acceptable.

Maximum Input Frequency—Routed to DStarA[28]	1 GHz
Maximum Input Frequency—Routed to FPGA[29]	200 MHz
Output Characteristics	
Differential Output Voltage into 100 ohm differential load (at DC)	600 mV_{pp} typical
Output Common Mode Voltage	1.125 V to 1.375 V
Maximum Output Frequency—Sourced from Cross Point Switch[30]	1 GHz
Maximum Output Frequency—Sourced from FPGA[31]	200 MHz
Differential Rise and Fall Time	180 ps, typical

The following figure shows the representative LVDS output operating at 100 MHz. 1 unit interval in this figure equals 5 ns.

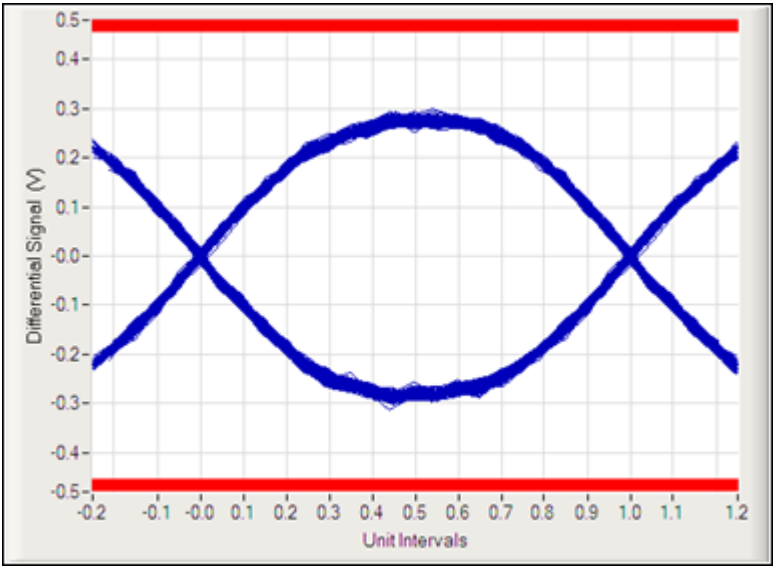
[28] Operation beyond 1 GHz is possible but performance is not guaranteed.
[29] Operation beyond 200 MHz is possible but performance is not guaranteed. This limitation comes from the FPGA, not the LVDS receiver.
[30] Operation beyond 1 GHz is possible but performance is not guaranteed.
[31] Operation beyond 200 MHz is possible but performance is not guaranteed. This limitation comes from the FPGA, not the LVDS driver.

Figure 13. Representative LVDS output operating at 100 MHz



The following figure shows the representative LVDS output operating at 1 GHz. 1 unit interval in the figure equals 500 ps.

Figure 14. Representative LVDS Output Operating at 1 GHz



PXI-Triggers

I/O Voltage Level	3.3 V CMOS, 5 V input tolerant

PXI-Star

I/O Voltage Level	3.3 V CMOS, 5 V input tolerant

PXIe-DStarB

The PXIe-DStarB signals are LVDS signals that allow the PXIe-6674T to route high speed trigger signals to any other PXIe slot in a chassis. Each PXI Express slot in a chassis has its own PXIe-DStarB connection with the System Timing Slot.

By default, these are driven logic low until configured by software.

Maximum operating frequency	200 MHz

PXIe-DStarC

The PXIe-DStarC signals are LVDS signals that come from other PXI Express slots in a chassis. Each PXI Express slot in a chassis has a PXIe-DStarC connection with the System Timing Slot. These allow other modules in a PXIe-Chassis to share a trigger or clock signal with the PXIe-6674T. The PXIe-6674T can connect a signal received through PXIe-DStarC to the PXIe-DStarA network (when sharing a clock signal) or treat the PXIe-DStarC as a trigger source.

Maximum operating frequency when used with the PXIe-DStarA network	1 GHz
Maximum operating frequency when used for triggering	200 MHz

Trigger Timing

Table 5. Asynchronous Trigger Delays and Skew Values

Trigger Source	Trigger Destination	Typical Delay[32]	Typical Skew[33]
Single Ended PFI	Single Ended PFI	23.4 ns	< .5 ns
Single Ended PFI	LVDS PFI	22.4 ns	< .5 ns
Single Ended PFI	PXI-Trigger	38.7 ns	< 1.5 ns
Single Ended PFI	PXI-Star	26.8 ns	< .75 ns
Single Ended PFI	PXIe-DStarB	23.2 ns	< .5 ns
LVDS PFI	Single Ended PFI	13.7 ns	< .5 ns
LVDS PFI	LVDS PFI	11.8 ns	< .5 ns
LVDS PFI	PXI-Trigger	28.9 ns	< 1.5 ns
LVDS PFI	PXI-Star	17.5 ns	< .75 ns
LVDS PFI	PXIe-DStarB	13.8 ns	< .5 ns
PXI-Trigger	Single Ended PFI	17.8 ns	< .5 ns
PXI-Trigger	LVDS PFI	16.6 ns	< .5 ns
PXI-Trigger	PXI-Trigger	33.8 ns	< 1.5 ns
PXI-Trigger	PXI-Star	21.0 ns	< .75 ns
PXI-Trigger	PXIe-DStarB	15.9 ns	< .5 ns
PXI-Star	Single Ended PFI	17.0 ns	< .5 ns
PXI-Star	LVDS PFI	15.6 ns	< .5 ns
PXI-Star	PXI-Trigger	26.2 ns	< 1.5 ns
PXI-Star	PXI-Star	20.2 ns	< .75 ns

[32] Typical Delay is measured from the input to the PXIe-6674T at the connector to the output at the connector. For example, Single Ended PFI to PXI-Star is the delay from the Single Ended PFI SMA connector to the PXI-Star at the backplane connector.

Table 5. Asynchronous Trigger Delays and Skew Values (Continued)

Trigger Source	Trigger Destination	Typical Delay[32]	Typical Skew[33]
PXI-Star	PXIe-DStarB	16.0 ns	< .5 ns
PXIe-DStarC	Single Ended PFI	13.6 ns	< .5 ns
PXIe-DStarC	LVDS PFI	7.2 ns	< .5 ns
PXIe-DStarC	PXI-Trigger	28.1 ns	< 1.5 ns
PXIe-DStarC	PXI-Star	16.8 ns	< .75 ns
PXIe-DStarC	PXIe-DStarB	13.0 ns	< .5 ns

Table 6. Synchronized Trigger PXI_Clk10 to Out

Trigger Destination	Clock to Out Time[34]
Single Ended PFI	11.2 ns Typical, 19.9 ns Max
LVDS PFI	9.8 ns Typical, 14.8 ns Max
PXI-Trigger	28.2 ns Typical, 30.2 ns Max
PXI-Star	14.8 ns Typical, 24.5 ns Max
PXIe-DStarB	9.4 ns Typical, 14.0 ns Max

[32] Typical Delay is measured from the input to the PXIe-6674T at the connector to the output at the connector. For example, Single Ended PFI to PXI-Star is the delay from the Single Ended PFI SMA connector to the PXI-Star at the backplane connector.

[33] Typical Skew is defined as the difference in arrival time of a rising edge on a common source to two or more outputs with in a trigger destination, as seen as the connector. For example, if Single Ended PFI(0) is asynchronously routed to all PXI-Star lines, the typical skew would be less than .75 ns.

[34] Clock to Out Time is the amount of time it takes for a logic change on a synchronous trigger to appear (at the connector) with respect to the rising edge of PXI-Clk10 (at the backplane connector) that it is synchronized to. Refer to the Synchronous Routing section of Chapter 3, Hardware Overview, for more information.

Table 7. Synchronized Trigger Setup and Hold Timing With Respect to PXI_Clk10

Trigger Source	Trigger Destination	Setup Time[35]	Hold Time[36]
Single Ended PFI	Single Ended PFI	11.2 ns Typical, 13.2 ns Max	-8.2 ns Typical, 1.1 ns Max
Single Ended PFI	LVDS PFI	11.2 ns Typical, 13.5 ns Max	-8.5 ns Typical, 0.8 ns Max
Single Ended PFI	PXI-Trigger	11.3 ns Typical, 14.2 ns Max	-7.5 ns Typical, 1.3 ns Max
Single Ended PFI	PXI-Star	11.2 ns Typical, 13.1 ns Max	-6.9 ns Typical, 2.0 ns Max
Single Ended PFI	PXIe-DStarB	13.2 ns Typical, 15.4 ns Max	-9.8 ns Typical, -0.4 ns Max
LVDS PFI	Single Ended PFI	0.6 ns Typical, 4.0 ns Max	0.4 ns Typical, 3.9 ns Max
LVDS PFI	LVDS PFI	-0.3 ns Typical, 4.3 ns Max	1.2 ns Typical, 3.5 ns Max
LVDS PFI	PXI-Trigger	-0.2 ns Typical, 3.6 ns Max	1.1 ns Typical, 5.0 ns Max
LVDS PFI	PXI-Star	-0.1 ns Typical, 3.7 ns Max	1.4 ns Typical, 5.0 ns Max
LVDS PFI	PXIe-DStarB	2.1 ns Typical, 5.7 ns Max	-0.5 ns Typical, 2.6 ns Max
PXI-Trigger	Single Ended PFI	11 ns Typical, 17.5 ns Max	-9.5 ns Typical, -4.8 ns Max
PXI-Trigger	LVDS PFI	10.9 ns Typical, 18.1 ns Max	-9.8 ns Typical, -5.4 ns Max

[35] Setup Time is the amount of time before a rising edge of PXI-Clk10 (at the backplane connector) that a logic level must be valid on the trigger source (at the connector) in order for the trigger destination to update. Refer to the Synchronous Routing section of Chapter 3, Hardware Overview, for more information.

Table 7. Synchronized Trigger Setup and Hold Timing With Respect to PXI_Clk10 (Continued)

Trigger Source	Trigger Destination	Setup Time[35]	Hold Time[36]
PXI-Trigger	PXI-Trigger	10.1 ns Typical, 17.0 ns Max	-7.8 ns Typical, -3.6 ns Max
PXI-Trigger	PXI-Star	9.7 ns Typical, 16.2 ns Max	--7.4 ns Typical, -3.1 ns Max
PXI-Trigger	PXIe-DStarB	10.7 ns Typical, 17.8 ns Max	-9.0 ns Typical, -5.1 ns Max
PXI-Star	Single Ended PFI	3.9 ns Typical, 10.9 ns Max	-2.5 ns Typical, -0.5 ns Max
PXI-Star	LVDS PFI	3.9 ns Typical, 11.1 ns Max	-3.1 ns Typical, -0.8 ns Max
PXI-Star	PXI-Trigger	2.7 ns Typical, 9.9 ns Max	-0.9 ns Typical, 0.9 ns Max
PXI-Star	PXI-Star	2.0 ns Typical, 9.6 ns Max	-0.1 ns Typical, 1.1 ns Max
PXI-Star	PXIe-DStarB	4.3 ns Typical, 11.7 ns Max	-2.4 ns Typical, -1.1 ns Max
PXIe-DStarC	Single Ended PFI	0.5 ns Typical, 3.9 ns Max	0.4 ns Typical, 3.7 ns Max
PXIe-DStarC	LVDS PFI	-0.3 ns Typical, 4.4 ns Max	0.5 ns Typical, 3.1 ns Max
PXIe-DStarC	PXI-Trigger	-1.1 ns Typical, 2.8 ns Max	1.9 ns Typical, 5.2 ns Max

[35] Setup Time is the amount of time before a rising edge of PXI-Clk10 (at the backplane connector) that a logic level must be valid on the trigger source (at the connector) in order for the trigger destination to update. Refer to the Synchronous Routing section of Chapter 3, Hardware Overview, for more information.

Table 7. Synchronized Trigger Setup and Hold Timing With Respect to PXI_Clk10 (Continued)

Trigger Source	Trigger Destination	Setup Time[35]	Hold Time[36]
PXIe-DStarC	PXI-Star	-0.5 ns Typical, 3.2 ns Max	3.1 ns Typical, 4.9 ns Max
PXIe-DStarC	PXIe-DStarB	1.3 ns Typical, 5.6 ns Max	0.2 ns Typical, 2.4 ns Max

FPGA Functionality

Trigger Routing

The following figure shows the routes that can be made.

[35] Setup Time is the amount of time before a rising edge of PXI-Clk10 (at the backplane connector) that a logic level must be valid on the trigger source (at the connector) in order for the trigger destination to update. Refer to the Synchronous Routing section of Chapter 3, Hardware Overview, for more information.

[36] Hold Time is the amount of time after a rising edge of PXI-Clk10 (at the backplane connector) that a logic level must be valid on the trigger source (at the connector) in order for the trigger destination to update. Refer to the Synchronous Routing section of Chapter 3, Hardware Overview, for more information.

[36] Hold Time is the amount of time after a rising edge of PXI-Clk10 (at the backplane connector) that a logic level must be valid on the trigger source (at the connector) in order for the trigger destination to update. Refer to the Synchronous Routing section of Chapter 3, Hardware Overview, for more information.

Figure 15. PXIe-6674T Routing Table

Sources		Destinations								
		Front Panel			Backplane					Onboard
		CLK OUT	PFI <0..5>	PFI LVDS <0..2>	PXI CLK 10 IN	PXI Star Trigger <0..16>	PXI TRIG <0..7>	DSTARA <0..16>	DSTARB <0..16>	OCXO Ref PLL
Front Panel	CLK IN	✓	✓†	✓†	✓	✓†	✓†	✓	✓†	✓
	PFI<0..5>		✓	✓		✓	✓		✓	
	PFI LVDS <0..2>		✓	✓		✓	✓	✓	✓	
Backplane	PXI CLK 10	✓	✓†	✓†		✓†	✓†		✓†	
	PXI CLK 100	✓	✓†	✓†		✓†	✓†		✓†	
	PXI STAR <0..16>		✓	✓		✓	✓		✓	
	PXI TRIG <0..7>		✓	✓		✓	✓		✓	
	DSTARC <0..16>		✓	✓		✓	✓	✓	✓	
Onboard	OCXO	✓	✓†	✓†	✓	✓†	✓†		✓†	
	Clock Gen	✓	✓†	✓		✓†	✓†	✓	✓†	
	Global Software Trigger		✓	✓		✓	✓		✓	

† Routing PXI_CLK10, PXIe_CLK100, OCXO or ClkGen is accomplished by setting the synchronization clock (using the NI-Sync Property Node) to the desired clock source and then routing the synchronization clock as the source.

Route through the FPGA.

Route to PFI LVDS can be made through the FPGA when used as a trigger, or through the PXIe-DSTARA network when used as a clock.

Frequency Measurement

Maximum Measurable Frequency[37]	200 MHz
Reference Counter Source[38]	PXIe_Clk100
Frequency Counter Sources	All Trigger inputs plus Clock In and the OCXO

37 Operation beyond 200 MHz is possible but performance is not guaranteed.

38 Accuracy of frequency measurement is relative to the frequency accuracy of the reference counter source. The Frequency Measure node in NI-Sync does not account for error from the reference source.

Trigger Sync Clock

Two independent synchronization clock zones:

- Front Synchronization Clock for PFI Single Ended and PFI LVDS
- Rear Synchronization Clock for PXI-Star, PXI-Trigger, and PXIe-DStarB

Synchronization Clock Sources	PXI_Clk10, PXIe_Clk100, Clock In, OCXO, and Clock Generation

Two division ratios can be specified in powers of 2 from 2 to 512. These ratios are used in all synchronization clock zones to divide down the selected full speed synchronization clock.

Physical

Chassis requirement	One 3U PXI Express slot (system timing slot)
Front panel connectors	Eight SMA female, 50 Ω
Front panel indicators	Two tricolor LEDs (green, red, and amber)
Weight	349 g (12.3 oz)
Dimensions (not including connectors)	16 cm × 10 cm (6.3 in. × 3.9 in.)

Power Requirements

Caution You can impair the protection provided by the PXIe-6674T if you use it in a manner not described in this document.

+3.3 V	2.54 A, max
+12 V	2.25 A, max
+5 V_{AUX}	0 A, max

Environmental

Maximum altitude	2,000 m (800 mbar) (at 25 °C ambient temperature)
Pollution Degree	2

Indoor use only.

Operating Environment

Ambient temperature range	0 to 55 °C (Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2. Meets MIL-PRF-28800F Class 3 low temperature limit and MIL-PRF-28800F Class 2 high temperature limit.)
Relative humidity range	10% to 90%, noncondensing (Tested in accordance with IEC-60068-2-56.)

Storage Environment

Ambient temperature range	-40 to 71 °C (Tested in accordance with IEC-60068-2-1 and IEC-60068-2-2. Meets MIL-PRF-28800F Class 3 limits.)
Relative humidity range	5% to 95%, noncondensing (Tested in accordance with IEC-60068-2-56.)

Shock and Vibration

Operating Shock	30 g peak, half-sine, 11 ms pulse (Tested in accordance with IEC-60068-2-27. Meets MIL-PRF-28800F Class 2 limits.)
Random Vibration	
Operating	5 to 500 Hz, 0.3 g_{rms}
Nonoperating	5 to 500 Hz, 2.4 g_{rms} (Tested in accordance with IEC-60068-2-64. Nonoperating test profile exceeds the requirements of MIL-PRF-28800F, Class 3.)

Safety Compliance Standards

This product is designed to meet the requirements of the following electrical equipment safety standards for measurement, control, and laboratory use:

- IEC 61010-1, EN 61010-1
- UL 61010-1, CSA C22.2 No. 61010-1

Note For UL and other safety certifications, refer to the product label or the *Product Certifications and Declarations* section.

Electromagnetic Compatibility

This product meets the requirements of the following EMC standards for electrical equipment for measurement, control, and laboratory use; for radio equipment; and for telecommunication terminal equipment:

- EN 61326-1 (IEC 61326-1): Class A emissions; Basic immunity
- EN 55011 (CISPR 11): Group 1, Class A emissions
- AS/NZS CISPR 11: Group 1, Class A emissions
- FCC 47 CFR Part 15B: Class A emissions
- ICES-001: Class A emissions

Note In the United States (per FCC 47 CFR), Class A equipment is intended for use in commercial, light-industrial, and heavy-industrial locations. In Europe, Canada, Australia and New Zealand (per CISPR 11) Class A equipment is intended for use only in heavy-industrial locations.

Note Group 1 equipment (per CISPR 11) is any industrial, scientific, or medical equipment that does not intentionally generate radio frequency energy for the treatment of material or inspection/analysis purposes.

Note To ensure the specified EMC performance, operate this product only with double-shielded cables and accessories (for example, RG-223 cables).

Notice For EMC declarations and certifications, and additional information, refer to the *Product Certifications and Declarations* section.

CE Compliance CE

This product meets the essential requirements of applicable European Directives, as follows:

- 2014/35/EU; Low-Voltage Directive (safety)
- 2014/30/EU; Electromagnetic Compatibility Directive (EMC)
- 2011/65/EU; Restriction of Hazardous Substances (RoHS)
- 2014/53/EU; Radio Equipment Directive (RED)
- 2014/34/EU; Potentially Explosive Atmospheres (ATEX)

Product Certifications and Declarations

Refer to the product Declaration of Conformity (DoC) for additional regulatory compliance information. To obtain product certifications and the DoC for NI products, visit *ni.com/product-certifications*, search by model number, and click the appropriate link.

Environmental Management

NI is committed to designing and manufacturing products in an environmentally responsible manner. NI recognizes that eliminating certain hazardous substances from our products is beneficial to the environment and to NI customers.

For additional environmental information, refer to the *Commitment to the Environment* web page at *ni.com/environment*. This page contains the environmental regulations and directives with which NI complies, as well as other environmental information not included in this document.

Waste Electrical and Electronic Equipment (WEEE)

EU Customers At the end of the product life cycle, all NI products must be disposed of according to local laws and regulations. For more information about how to recycle NI products in your region, visit *ni.com/environment/weee*.

电子信息产品污染控制管理办法（中国 RoHS）

中国客户 National Instruments 符合中国电子信息产品中限制使用某些有害物质指令(RoHS)。关于 National Instruments 中国 RoHS 合规性信息，请登录 `ni.com/environment/rohs_china`。(For information about China RoHS compliance, go to `ni.com/environment/rohs_china`.)

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